REMARKS

Examiner Thomas L. Dickey is thanked for his examination of the subject Patent Application. The Specification, Drawings and Claims have been carefully reviewed with respect to the cited prior art and the Claims have been amended and are considered to be in condition for Allowance.

Claim Status

Claims 1-3, 5 and 6 remain in this application.

Detailed Action Item 1

Examination Continued Under 37 CFR 1.114

1. Applicant's submissions filed on 9 September 2003 are acknowledged as having been entered.

Detailed Action Item 2

Claim Rejections - 35 USC § 112

Reconsideration of the rejection of Claims 1, 2, 5 and 6 under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement, is respectfully requested based on the following:

The Examiner writes:

> Claims 1,2,5, and 6 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement.
>
> The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the

> inventor(s), at the time the application was filed, had possession of the claimed invention. These claims all require that the top surface comprise more than five (5) individually connected top surfaces defined by multiple regions of individual cross-sectional shapes, thus excluding top surfaces comprising one, two, three, four, or five individually connected top surfaces. The application as filed discloses that applicants considered their invention to include any number of individually connected top surfaces, so long as that number exceeds one. Note application, page 14, line 19, through page 15, line 4. Applicants are not free now to set an arbitrary minimum number of individually connected top surfaces unless that number was disclosed in the application as filed. The only minimum number of individually connected top surfaces disclosed, in the application as filed, was two.

The Applicant responds:

The specification at page 14, line 19 through page 15, line 4 reads:

> It will be observed that the surface of the first polysilicon layer exposed in (125) can be "folded" several times over by having several steps or "fins" similar to that is found in heat sinks. Furthermore, the fins can comprise other shapes, such as triangular, or trapezoidal, and so on, all designed to increase the surface area. As another key step, additional area is gained by removing oxide spaces (155) to expose additional polysilicon areas underneath the spacers, as seen in Fig. 2g.

This passage refers to Fig. 2g which shows the simplest of the possible folded configurations. Please note that the surface of the polysilicon 120 in question is that which is under the oxide 160. That surface has an elevated horizontal left hand piece, a vertical left hand wall, a lower central horizontal piece, a vertical right hand wall and an elevated horizontal right hand piece. That makes five (5) folded surfaces. Therefore, the specification in the simplest construction according to the method teaches a folded five surface as the minimum.

To have a possible three or four folded surface (using the spacer technique) would require dishing out the polysilicon with an isotropic etch perhaps. To have a two folded surface (using the spacer technique) does not seem possible. To have a one folded surface (using the spacer technique) would require not etching the polysilicon having spent the effort making unused

expendable spacers.

To have more than five (say, rectangular) surfaces is disclosed in the specification by speaking of "heat sink fins". In the case of one extra fin placed in the Fig. 2g or Fig. 2h, there would be three elevated surfaces, two lower surfaces and four vertical surfaces. It is the vertical surfaces that add to the coupling capability. The more "fins", the more vertical surfaces, the more the coupling. In this one "fin" configuration, the folded surface count would be nine.

Allowing for different etching techniques on different mask material combinations and on patterns in the original photo resist, multiple "fins" of rectangular, triangular or trapezoidal shapes are possible.

The Applicant has provided a method to produce a simple folded floating gate structure using spacers to form "steps" as shown in the figures and discloses that this technique does not end there. The Applicant is disclosing that this technique can result in more complex surfaces resulting in greater coupling and thus other structures as claimed.

The number (five) is obvious from the figures and the specification. The numbers (one and two) do not make sense in this context. The numbers (three and four) would be an etching controlled variation of five folded surface case, but perhaps not yielding the maximum coupling. Numbers greater than five are possible.

Detailed Action Item 3

Claim Rejections - 35 USC §102

Reconsideration of the rejection of Claim 1 under 35 U,S,C. 102(a) as being anticipated by Nishihara (5,854,502) is respectfully requested based on the following reasons.

The Examiner writes:

> Nishihara discloses a stacked-gate flash memory cell comprising a semiconductor substrate 1 having an active area (seen directly below thin gate oxide film region 17), a floating Poly-Si gate 25 with a bottom surface and a multiply connected top surface, the bottom surface being flat and overlying the active area, the multiply connected top surface overlying the bottom surface; the multiply connected top surface being defined by multiple regions of individual cross-sectional shapes, wherein the area of the multiply connected top surface overlying the active area is greater than the area of the bottom surface, wherein the individual cross-sectional shapes are selected from a group consisting of rectangular, trapezoidal and triangular shapes (in this case, rectangular or triangular), said multiply connected top surface comprising nine (9) individually connected top surfaces, which is more than five (5) individually connected top surfaces defined by said multiple regions of individual cross-sectional shapes, a conformal inter-poly dielectric layer 27 replicating the individual cross-sectional shapes over the floating Poly-Si gate 25; and a conformal Poly-Si control gate 26 replicating the individual cross-sectional shapes over the inter-poly dielectric layer 27. Note figure 7B and column 5 lines 34-54 of Nishihara.

The Applicant responds:

Nishihara provides a floating gate that is double gull-winged in shape and not only overlies the channel area (active area) but also extends a distance beyond the channel area. This is due to the method of construction.

The doping to form the channel apparently occurs prior to the formation of the floating gate. This contrasts with the instant method which defines the channel by forming source and drain regions after forming the floating gate and the control gate.

Indeed, the Nishihara coupling between the control gate and the floating gate is comparatively large and is only due to its overall extent which goes well

beyond the channel region. The gull-wing (the sloped portions) shape may contribute some small additional coupling, but that is not specified and results only from the constant thickness floating gate necessarily being conformal to the gate oxide over the channel and the thickened oxides beyond the channel.

There are nine folded surfaces as observed by the Examiner. However, in the region directly over the channel, there are only three folded surfaces. Please refer to attached Illustration 1, an enlargement of Fig. 7B. Then look at Illustration 2 which details the region over the channel. This illustrates a left sloped surface, a center horizontal surface and a right sloped surface. Illustration 3 shows how Nishihara's structure would have to be modified in order for it to be described with a nine folded surface in the manner of the instant structure.

By contrast, in the instant case, both the floating gate and the control gate are contained within the span of the channel region formed by the source and drain region which are formed after the floating gate, polyoxide and control gate are formed. In this manner, the instant cell and its components require the smallest of real estate. Having been made small, the coupling between the control gate and the floating gate then must be enhanced significantly and that is the novelty of the instant invention and it resulting structure

It is with this description, Claim 1 is now amended.

Detailed Action Item 4

Claim Rejections - 35 USC § 103

Reconsideration of the rejections of Claims 2,5, and 6 under 35 U.S.C. 1 03(a) as being unpatentable over Nishihara (5,859,454) in view of MURAI (5,243,559) is respectfully requested.

The Examiner writes:

> Nishihara discloses a stacked-gate flash memory cell with all the limitations of claims I. 2,5, and 6 except certain specific dimensions for the thickness of the floating gate (190-210 nm), an ONO inter-poly dielectric layer (15-25 nm), and control gate (150-200 nm).
>
> Note figure 6 of Nishihara. Nishihara is silent on whether the interpoly layer should be made of and the question of what the floating gate, control gate, and interpoly layer dimensions should be. However, Murai, which was published well before Nishihara was applied for, and would have been well known to Nishihara, discloses a stacked-gate flash memory cell with a floating gate 36 having a thickness in the range of 190-210 nm, an aNa inter-poly dielectric layer 37 having a thickness in the range of 15-25 nm, and a control gate 38 having a thickness in the range of 150-200 nm. Note column 4 lines 37, 43, and 50 of Murai. Therefore, it would have been obvious to a person having skill in the art to build a physical realization of Nishihara's stacked-gate flash memory cell using the dimensions taught by Murai in order to build Nishihara's stacked-gate flash memory cell with a minimum of experimentation. In the absence of specific instructions from Nishihara one having skill in the art would reasonably believe that any dimensions known to Nishihara (such as the Murai dimensions) would work.

The Applicant responds:

> Claims 2, 5 and 6 are dependent on newly amended Claim 1.

Detailed Action Item 5

Response to Arguments

The Examiner writes:

> 5. Applicant's arguments filed 12/30/02 with respect to claims 1-6 have been considered but are moot in view of the new ground(s) of rejection. With regard to the new art it should be noted that Nishihara meets the claims by disclosing a floating gate having, inter alia, a flat bottom, but Nishihara does not disclose a floating gate whose bottom is entirely flat, as shown in applicant's figures 2h-21.

The Applicant agrees with the Examiner that the entire bottom surface of Nishihara's floating gate is not flat. Amended Claim 1 addresses this point either directly or indirectly.

Detailed Action Item 6

Allowable Subject Matter

The Examiner writes:

> 6. Claim 3 is allowed over the references of record because none of these references disclosed or can be combined to yield the claimed invention such as a stacked-gate flash memory cell having a floating Poly-Si gate with multiply connected surfaces of individual shapes comprising: a semiconductor substrate having an active area; a floating Poly-Si gate with a bottom surface and a multiply connected top surface; said bottom surface being flat and overlying said active area; said multiply connected top surface overlying said bottom surface; said multiply connected top surface being defined by multiple regions of individual cross-sectional shapes, wherein the area of said multiply connected top surface overlying said active area is greater than the area of said bottom surface; wherein said individual cross-sectional shapes are selected from a group consisting of rectangular, trapezoidal and triangular shapes; a conformal inter-poly dielectric layer replicating said individual cross-sectional shapes over said floating Poly-Si gate; and a conformal Poly-Si control gate replicating said individual cross-sectional shapes over said inter-poly dielectric layer, wherein said regions of individual cross-sectional shapes have a depth between about 900 to 1000 A.

The Applicant respectfully accepts this allowance.

CONCLUSION

We have reviewed the related art references made of record and agree with Examiner Dickey that none of these suggest the present claimed invention.

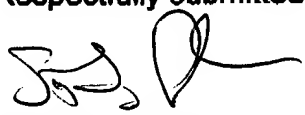
In light of the above arguments, it is suggested that the Claims now clearly describes the invention. All claims are therefore believed to be in condition for

allowance.

Allowance of all claims is therefore respectfully requested.

It is requested that should Examiner Dickey not find that the Claims are now Allowable that the Examiner call the undersigned attorney at 845-452-5863 to overcome any problems preventing allowance.

Respectfully submitted,



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